L Number	Hits	Search Text	DB	Time stamp
1	32	(different with width) same (spacers or spacer or sidewall or sidewalls) same transistor	USPAT; US-PGPUB	2004/08/18 08:43
2	19	((different with width) same (spacers or spacer or sidewall or sidewalls) same transistor) and @ad<20000518	USPAT; US-PGPUB	2004/08/18 08:57
3	9	(different with width) same (spacers or spacer or sidewall or sidewalls) same transistor	EPO; JPO; DERWENT; IBM_TDB	2004/08/18 08:55
4	2	(different with width) same (spacers or spacer or sidewall or sidewalls) and CMOS	EPO; JPO; DERWENT; IBM_TDB	2004/08/18 08:57
5	76	(different with width) same (spacers or spacer or sidewall or sidewalls) and CMOS	USPAT; US-PGPUB	2004/08/18 09:10
6	30	((different with width) same (spacers or spacer or sidewall or sidewalls) and CMOS) and @ad<20000518	USPAT; US-PGPUB	2004/08/18 09:10
7	17	(((different with width) same (spacers or spacer or sidewall or sidewalls) and CMOS) and @ad<20000518) not (((different with width) same (spacers or spacer or sidewall or sidewalls) same transistor) and @ad<20000518)	USPAT; US-PGPUB	2004/08/18 08:57
8	2360	(width) same (spacers or spacer or sidewall or sidewalls) and CMOS	USPAT; US-PGPUB	2004/08/18 09:10
9	1562	(width with (spacers or spacer or sidewall or sidewalls))and CMOS	USPAT; US-PGPUB	2004/08/18 09:10
10	949	((width with (spacers or spacer or sidewall or sidewalls))and CMOS) and @ad<20000518	USPAT; US-PGPUB	2004/08/18 09:11
11	862	(((width with (spacers or spacer or sidewall or sidewalls))and CMOS) and @ad<20000518) and etching	USPAT; US-PGPUB	2004/08/18 09:11
12	805	((((width with (spacers or spacer or sidewall or sidewalls))and CMOS) and @ad<20000518) and etching) and (gate or electrode)	USPAT; US-PGPUB	2004/08/18 09:12

US-PAT-NO: 5994743

DOCUMENT-IDENTIFIER: US 5994743 A

TITLE: Semiconductor device having different sidewall widths and different source/drain depths for NMOS & PMOS structures

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Abstract Text - ABTX (1):

A CMOS device includes a first conductive type channel MOSFET having first side-wall spacers on side surfaces and having a source and drain region of an LDD structure, and a second conductive type channel MOSFET having second side-wall spacers on side surfaces and having a source and drain region of a single drain structure, wherein a **width** of the first side-wall spacers is larger than that of the second side-wall spacers, restraining the short channel effect and hot carrier effect as well.

Brief Summary Text - BSTX (13):

That is, The document of Japanese Laid-Open Patent Application No. Hei3-41763 discloses the following process: a gate electrode is formed on an nMOSFET forming region and a pMOSFET forming region and n.sup.- -type region is formed in the nMOSFET forming region with a resist film coated on the pMOSFET forming region; side-wall spacers are formed on the side surfaces of gate electrode for the nMOSFET and an n-type impurity is doped into the nMOSFET forming region in high concentration to form an n.sup.+ -type region with a resist film coated on the pMOSFET forming region; and other

side-wall **spacers,**
width of which is wider than that of nMOSFET, are formed on the side surfaces
of gate electrode of the pMOSFET forming region and a p-type impurity is doped
into the pMOSFET forming region in high concentration to form a p.sup.+ -type
source and drain region with a resist film coated on the nMOSFET forming
region.

Brief Summary Text - BSTX (15):
According to the examples described above, the nMOSFET is formed of the LDD
structure while the pMOSFET is formed of the single drain structure as shown in
FIG. 3 (f). However, since the short channel effect depends on a junction
depth of the source and drain regions located close to the channel region in
general, in the examples described above, the nMOSFET region is controlled by
the short channel characteristic depending on a junction depth of the n-type
low concentration region 109 and the pMOSFET region is controlled by that
characteristic depending on a junction depth of the p-type high concentration
source and drain region 115. Therefore, since the n-type low concentration
region 109 should remain to a certain extent in the nMOSFET forming region, it
is desirable that the side-wall spacers 111, which become masks in the
ion-implantation of As.sup.+ shown in FIG. 3(f), are formed thick in
consideration of the **width** in a lateral direction of the n-type high
concentration region 119. However, since the pMOSFET side is used by the
process to be inverted by the ion-implantation of B.sup.+ as shown in FIG. 3(e)
after forming a conductive type of the n-type low concentration region as
side-wall spacers, the p-type high concentration source and drain region should
be formed to some extent of depth in case of forming the

side-wall spacers in
thick. To this end, the junction depth of the p-type high concentration source
and drain region in the pMOSFET region becomes deeper than that of the n-type
high concentration source and drain region in the nMOSFET region. As a result,
the short channel effect of the pMOSFET becomes remarkable, so that the
critical dimension of the gate length for the pMOSFET is limited.

Brief Summary Text - BSTX (18):
According to a first aspect of the present invention, there is provided a
CMOS device including: a first conductive type channel MOSFET having first
side-wall spacers on side surfaces thereof and having a source and drain region
of an LDD structure; and a second conductive type channel MOSFET having second
side-wall spacers on side surfaces thereof and having a source and drain region
of a single drain structure, in which a **width** of the first side-wall spacers is
larger than that of the second side-wall spacers.

Brief Summary Text - BSTX (20):
In the process of manufacturing a CMOS device for forming nMOSFET of the LDD
structure and pMOSFET of the single drain structure, since the ion-implantation
is carried out to form the p-type source and drain region after forming the
side-wall spacers of the pMOSFET, **width** of which is smaller than those of the
nMOSFET, the conductive type of n-type low concentration region (LDD structure)
can be inverted even if the source and drain region of pMOSFET may be
relatively shallow. Thus, the junction depth of the source and drain region in
pMOSFET can be made shallow or equal to that of the source and drain region in
nMOSFET, restraining the short channel effect of pMOSFET to achieve a fine or

critical dimension of device. Furthermore, the LDD structure (or n-type low concentration region) in the nMOSFET is sufficiently secured, restraining the short channel effect and hot carrier effect as well.

Detailed Description Text - DETX (9):

According to the manufacturing method described above, when forming the p.sup.+ -type source and drain region 11 in the case of pMOSFET, the **width** of side-wall spacers 8, 8 are made small, as shown in FIG. 1(f), therefore, the conductive type of n-type low concentration region 7 can be inverted without ion-implanting a p-type impurity thereon and making it deep. Thus, the junction depth of p.sup.+ -type source and drain region 11 can be made shallow, restraining the short channel effect. While in the case of nMOSFET, the **width** of side-wall spacers are made sufficiently larger to eventually form a desirable length of the n-type low concentration region 7 as an LDD structure region, restraining the short channel effect and hot-carrier effect as well.

Claims Text - CLTX (2):

a **width** of the first side-wall spacers is larger than that of the second side-wall spacers, and

Claims Text - CLTX (9):

wherein a **width** of the first side-wall spacers is larger than that of the second side-wall spacers; and a junction depth of the source and drain region in the first conductive type channel MOSFET is larger than that of the source and drain region in the second conductive type channel MOSFET.